IN THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) An apparatus for reducing a magnitude of a rate of current change of an integrated circuit, comprising:

a control stage that generates a control signal indicative of whether power consumption by the integrated circuit needs to be reduced; and

a counter stage that inputs the control signal and generates a plurality of signals to a plurality of transistors, wherein the plurality of signals sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current sourced from a power terminal to a ground terminal of the integrated circuit, and wherein the plurality of transistors and the control stage are arranged in parallel.

2. (Canceled)

3. (Currently Amended) The apparatus of claim 1, wherein the counter stage enables the plurality of transistors when power consumption by the integrated circuit does not need to be reduced.

4. (Original) The apparatus of claim 1, wherein the plurality of transistors are each one selected from the group consisting of a p-type transistor and a n-type transistor.

5. (Currently Amended) A circuit for reducing a rate of current change of a microprocessor, comprising:

a control stage that is connected to a power terminal and a ground terminal, wherein the control stage generates a control signal that is indicative of whether power consumption by the microprocessor needs to be reduced; and

a counter stage that inputs the control signal and a clock signal, wherein the counter stage is arranged to generate a plurality of signals to a plurality of transistors connected in parallel across the power terminal and the ground terminal, and wherein the plurality of transistors are arranged in parallel with the control stage,

wherein, dependent on the control signal, the plurality of signals are generated to sequentially disable the plurality of transistors to cause a gradual reduction in an amount of current sourced from the power terminal to the ground terminal by the plurality of transistors.

6-10. (Canceled)

11. (New) The circuit of claim 5, wherein the plurality of transistors, when in an enabled state, source substantially a maximum amount of current from the power terminal to the ground terminal.

REMARKS

Please reconsider the present application in view of the above amendments and the following remarks. Applicant thanks the Examiner for carefully considering the present application.

I. Disposition of Claims

Claims 1, 3-5, and 11 are currently pending in the present application. By way of this reply, claims 1 and 5 have been amended.

II. Claim Amendments

Claims 1 and 5 have been amended to clarify that the plurality of transistors and the control stage are arranged in parallel. No new matter has been added by way of these amendments as support for these amendments may be found, for example, in Figure 2a of the present application.

III. Rejection(s) Under 35 U.S.C § 102

Claims 1, 3-5, and 11 of the present application were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,424,669 issued to Teggatz et al. (hereinafter "Teggatz"). For the reasons set forth below, this rejection is respectfully traversed.

The present invention is directed to a technique for reducing the magnitude of current change when power consumption in an integrated circuit needs to be reduced. In prior art systems, when a power consumption reduction need arose in response to, for

example, over-heating, current is instantly decreased (*i.e.*, the magnitude of current change is high). *See* Specification, paragraph [0003]. Such instant reduction in current leads to high magnitudes of voltage reduction, which may cause integrated circuit damage. *See* Specification, paragraph [0003].

With reference to the exemplary embodiment of the present invention shown in Figure 2a of the present application, a circuit in accordance with the present invention causes a gradual reduction in current to occur in response to a power consumption reduction need. *See* Specification, paragraphs [0016], [0017]. When a power consumption reduction need arises, a control stage **30** generates a control signal **m_out** to a counter stage **32**, which, in turn, sequentially disables a plurality of transistors **34**, **36**, **38**, **40** to cause a gradual reduction in the amount of current sourced from V_{DD} **42** to V_{SS} **44**. *See* Specification, paragraphs [0016], [0017]. This gradual reduction in current is exemplarily shown in Figure 2b of the present application. In Figure 2b of the present application, the current sourced from V_{DD} **42** to V_{SS} **44** gradually decreases from 10 amperes to 5 amperes over time as the plurality of transistors **34**, **36**, **38**, **40** are sequentially disabled by signals $\mathbf{C_0}$, $\mathbf{C_1}$, $\mathbf{C_2}$, $\mathbf{C_3}$ generated by the counter stage **32**. *See* Specification, paragraphs [0015] – [0017].

Further, as shown in Figure 2a of the present application, the control stage **30** is arranged to be in parallel with the plurality of transistors **34**, **36**, **38**, **40**. In such an arrangement, the control stage **30** experiences (or "sees") the same voltage potential that is across the plurality of transistors **34**, **36**, **38**, **40**, thereby allowing the control stage **30** to directly monitor and respond to (via control signal **m_out**) the current being sourced from V_{DD} **42** to V_{SS} **44** through the plurality of transistors **34**, **36**, **38**, **40**. Accordingly,

independent claims 1 and 5 of the present application have been amended to clarify that the plurality of transistors and the control stage are arranged in parallel. Applicant notes that these amendments are clarifying in nature and are not believed to require any further search.

Teggatz, in contrast to the present invention, fails to disclose the limitations of the claimed invention discussed above. For example, as shown in Figure 2 of Teggatz, the purported control stage **21**, **23** *is not* in parallel with the purported plurality of transistors **27**, **29**, **31**, **33**. In other words, the voltage potential across the purported control stage **21**, **23** is not equal to the voltage potential across transistors **27**, **29**, **31**, **33** (due to the presence of load **45**). The purported control stage **21**, **23** therefore cannot directly monitor and respond to the amount of current sourced from VDD through the load **45** and the plurality of transistors **27**, **29**, **31**, **33** to ground. Thus, Teggatz fails to disclose, or otherwise teach, that its purported control stage is arranged in parallel with its purported plurality of transistors. Accordingly, Teggatz fails to disclose each and every limitation recited in amended independent claims 1 and 5 of the present application.

In view of the above, Teggatz fails to show or suggest the present invention as recited in amended independent claims 1 and 5 of the present application. Thus, amended independent claims 1 and 5 of the present application are patentable over Teggatz. Dependent claims are allowable for at least the same reasons. Accordingly, withdrawal of this rejection is respectfully requested.